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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,325	09/23/2005	Hiroshi Jiken	1110/95342	2064

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

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09/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,325	JIKEN ET AL.	
	Examiner	Art Unit	
	SAMUEL A. GEBREMARIAM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toeda JP, 06-163556A in view of Ikari et al., US patent No., 6,548,886.

Regarding claim 5, Toeda teaches (fig. 1) a semiconductor epitaxial wafer (fig. 1) having plural epitaxial layers (2,3) stacked on a semiconductor substrate (1), wherein: the plural epitaxial layers (2,3) are stacked on a front side (upper surface of 1) of the semiconductor substrate (1); and an impurity concentration of any one of the plural epitaxial layers (2) is high enough to afford a latch-up resistance (refer to the abstract) and a high-frequency conformity and is higher than impurity concentrations of the semiconductor substrate (1) and other ones of the plural epitaxial layers (3).

Toeda does not explicitly state that the semiconductor substrate is doped with nitrogen.

However it is conventional and also taught by Ikari to dope a silicon substrate with nitrogen in order to improve the gettering ability of the substrate (col. 20, lines 45-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a nitrogen doped semiconductor substrate as taught by Ikari in the structure of Toeda in order to improve the gettering ability of the substrate.

Regarding claim 6, Toeda teaches a semiconductor epitaxial wafer (fig. 1) having plural epitaxial layers (2,3) stacked on a semiconductor substrate (1), wherein: the plural epitaxial layers (2,3) are stacked on a front side of the semiconductor substrate (1); an impurity concentration of any one of the plural epitaxial layers (2) is high enough for the formation of a gettering site and is higher than impurity concentrations of the semiconductor substrate (1) and other ones of the plural epitaxial layers (3); and an impurity concentration of the semiconductor substrate (1) is at a level of suppressing impurity discharge from the semiconductor substrate (refer to the abstract).

Toeda does not explicitly state that the semiconductor substrate is doped with nitrogen.

However it is conventional and also taught by Ikari to dope a silicon substrate with nitrogen in order to improve the gettering ability of the substrate (col. 20, lines 45-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a nitrogen doped semiconductor substrate as taught by Ikari in the structure of Toeda in order to improve the gettering ability of the substrate.

Regarding claim 7, Toeda teaches substantially the entire claimed structure of claim 5 above including an impurity concentration of the epitaxial layer (2) being in contact with the semiconductor substrate (1) among the plural epitaxial layers (2,3) is

higher than the impurity concentrations of the semiconductor substrate (1) and the other epitaxial layers (3).

Regarding claim 10, Toeda teaches substantially the entire claimed structure of claim 5 above including a high-concentration epitaxial layer (2) among the plural epitaxial layers contains boron (refer to paragraph 0007 of the attached computer translation).

3. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toeda in view of Ikari and in further view of Asano et al., US2003/0197190.

Regarding claim 8, Toeda teaches a semiconductor epitaxial wafer having plural epitaxial layer (2,3) stacked on a semiconductor substrate (1), wherein: plural epitaxial layers (2,3) are stacked on a front side of the semiconductor substrate (1); an impurity concentration of a high-concentration epitaxial layer among the plural epitaxial layers is 8x1018 (atoms/cm3 refer to paragraph 0008).

Toeda does not explicitly teach that the semiconductor substrate is doped with nitrogen or an impurity concentration of the semiconductor substrate is $1.22x\ 10^{14}$ to $1.46x\ 10^{16}$ ($atoms/cm^3$).

However it is conventional and also taught by Ikari to dope a silicon substrate with nitrogen in order to improve the gettering ability of the substrate (col. 20, lines 45-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a nitrogen doped semiconductor substrate as taught by Ikari in the structure of Toeda in order to improve the gettering ability of the substrate.

Asano teaches the use of a semiconductor substrate (10) having an impurity concentration of $1x10^{14}$ to $1x10^{18}/cm^3$ in the structure of a semiconductor device with reduced parasitic capacitance.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the substrate taught by Asano in the modified structure of Toeda and Ikari in order to form a device with reduced parasitic capacitance.

Regarding claim 9, the combined structure of Toeda, Ikari and Asano teaches substantially the entire claimed structure of claim 8 above including a resistivity of a high-concentration epitaxial layer among the plural epitaxial layers is 0.002 to 0.1 (Ω-cm) (inherently the same); and a resistivity of the semiconductor substrate is 1 to 100 (Ω-cm, [0061], Asano).

Response to Arguments

4. Applicant's arguments with respect to claims 5-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/SAG/

August 27, 2008